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51472 7590 09/24/2007 GARLICK HARRISON & MARKISON P.O. BOX 160727 AUSTIN, TX 78716-0727			EXAMINER TORRES, JUAN A	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

09/729,443

Applicant(s)

JAFFE ET AL.

Examiner

Juan A. Torres

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 27 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 62-115 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 62-115 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 December 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Drawings***

The drawings are objected to because Figures 3 and 4 are of not enough quality; it is suggested to send new figures 3 and 4 in the same quality that figures 1 and 2 (see below). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

The modifications to the claims were received on 08/02/2007. These modifications are accepted by the Examiner.

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In view of the cancellation of all the previously presented claims 1-61 in the amendment filed on 08/02/2007, the Examiner withdraws claims objections to claims 33-42 and 44-46 of the previous Office action.

***Claim Rejections - 35 USC § 112***

The modifications to the claims were received on 08/02/2007. These modifications are accepted by the Examiner.

In view of the cancellation of all the previously presented claims 1-61 in the amendment filed on 08/02/2007, the Examiner withdraws claims rejections under 35 USC § 112 first paragraph to claims 1-3, 5-16, 18-20, 27-28, 30-42, 44-48, 50-54, 56-61 of the previous Office action.

In view of the cancellation of all the previously presented claims 1-61 in the amendment filed on 08/02/2007, the Examiner withdraws claims rejections under 35 USC § 112 second paragraph to claim 14 of the previous Office action.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 62-115 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification doesn't disclose "a third symbol" following the second symbol, and where this third symbol is coming from, a first trellis encoder a second trellis encoder, after the interleaver or the de-interleaver.

***Claim Rejections - 35 USC § 101***

The modifications to the claims were received on 08/02/2007. These modifications are accepted by the Examiner.

In view of the cancellation of all the previously presented claims 1-61 in the amendment filed on 08/02/2007, the Examiner withdraws claims rejections under 35 USC § 101 to claims 1-3, 5-16, 18-22, 24-28, 30-42, 44-48, 50-54, 56-61 of the previous Office action.

***Claim Rejections - 35 USC § 102***

The modifications to the claims were received on 08/02/2007. These modifications are accepted by the Examiner.

In view of the cancellation of all the previously presented claims 1-61 in the amendment filed on 08/02/2007, the Examiner withdraws claims rejections under 35 USC § 102 to claims 1-3, 5-8, 10-11, 15-16, 18-19, 21-22, 24-25, 27-28, 30-31, 33-36, 40-42, 44-45, 47-48, 50-51 and 53-54, 56-59 of the previous Office action.

***Claim Rejections - 35 USC § 103***

The modifications to the claims were received on 08/02/2007. These modifications are accepted by the Examiner.

In view of the cancellation of all the previously presented claims 1-61 in the amendment filed on 08/02/2007, the Examiner withdraws claims rejections under 35

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USC § 103 to claims 9, 13-14, 20, 38-39 and 46; and claims 12, 20, 26, 32, 37, 52 and 59-61 of the previous Office action.

### ***Other Considerations***

Carefully consideration has been done to the specification and drawings of the present Application. In an intent by the Examiner to bring clarity in the present Office action, the Examiner is including the "detail description of the invention" (with the exception of the last paragraph) and drawings, as well as the portions of the references that clearly support the rejections under 35 USC § 112, § 102 and § 103.

#### **DETAILED DESCRIPTION OF THE INVENTION**

Figure 1 is a graphical illustration of a communications system. In Figure 1, data 101 is provided to an encoder 103. The encoder codes the data and then provides it to a transmitter 105. The transmitter modulates the coded data on a carrier frequency, amplifies the resultant signal and broadcasts it to a relay satellite 107. The relay satellite 107 then rebroadcasts the data transmission to a receiver 109. The received signal is then provided by the receiver 109 to a mixer 113. A voltage controlled oscillator 123 provides a mixer signal to the mixer with the result that the coded signal is translated to a baseband signal. The coded baseband signal comprises the data and the coding added by encoder 103. The transport interface of the signal from (and including) the transmitter 105 to (and including) the receiver 109 is referred to as a channel 111.

The coded data from the multiplier 113 is filtered (filter not shown) and provided to a slicer 115. The slicer 115 extracts symbols from the coded data stream and provides it to a decoder 119. The decoder 119 decodes the symbols and creates a data stream 121. A phase detector 117 compares the symbol found by the slicer 115 with the value input to the slicer. By comparing the signal input to the slicer to the actual symbol found by the slicer in the phase detector 117, the phase detector detects whether the slicing process is leading or lagging the actual symbol value detected within the data stream. The phase detector 117 can then adjust the voltage controlled oscillator 123 to adjust the mixer signal provided to the multiplier 113 to match the carrier signal.

Figure 2 is a graphical illustration of a communication system in which the encoder 103 is replaced by a turbo encoder 200. The turbo encoder 200 accepts data 201. The data is then

encoded in a first trellis encoder 203. The data is also interleaved by an interleaver 205 and provided to a second trellis encoder 207. The second trellis encoder 207 may be identical to the first trellis encoder 203, but it may also be different. The outputs of trellis encoders 203 and 207 are then punctured by switch 209. In other words, switch 209 selects between the output of trellis encoder 203 and trellis encoder 207. The punctured output of turbo encoder 200 is then provided to a channel 211.

The signal received from the channel is then coupled into a multiplier 213, and the received signal is mixed with a mixer signal (as provided by the VCO 223), which replicates the carrier signal. The slicer 215 slices the symbols from the data stream, and the phase detector 217 detects the difference between the sliced symbol found at the output of the slicer 215 and the value input to the slicer. The output of the phase detector then adjusts the VCO 223 in order to correct the carrier signal being mixed in multiplier 213. The output of the slicer is then coupled into turbo decoder 219 to decode the turbo encoded data.

Turbo encoder 200 is a parallel concatenated encoder. Parallel concatenated codes ("turbo codes") allow communications systems to operate near the Shannon capacity. However, when operating in this region, the signal to noise ratio may be very low. This low signal to noise ratio ( $E_b/N_0$ ) can make synchronization with a received signal difficult. If the channel symbol error rate is greater than 1:10 (i.e., one out of ten transmitted signals is decoded incorrectly), a decision directed loop, such as illustrated in Figure 2 (comprising the slicer 215 and phase detector 217) can fail. In order to improve the accuracy, the slicer 215 may be replaced by a Viterbi decoder as illustrated in Figure 3. Viterbi decoders typically produce the most likely channel symbol based on past data, present data and (depending on trace-back depth) future data. A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer). In the embodiment illustrated in Figure 3, future data is not available, so the Viterbi decoder 301 will examine past and present data in order to produce a symbol, which is more likely to be accurate than one determined by a slicer mechanism such as illustrated in Figure 2. A Viterbi decoder is more likely to make an accurate decision as to what the symbol being decoded is based on a history of inputs than can a slicer, which makes a decision based on only the present input.

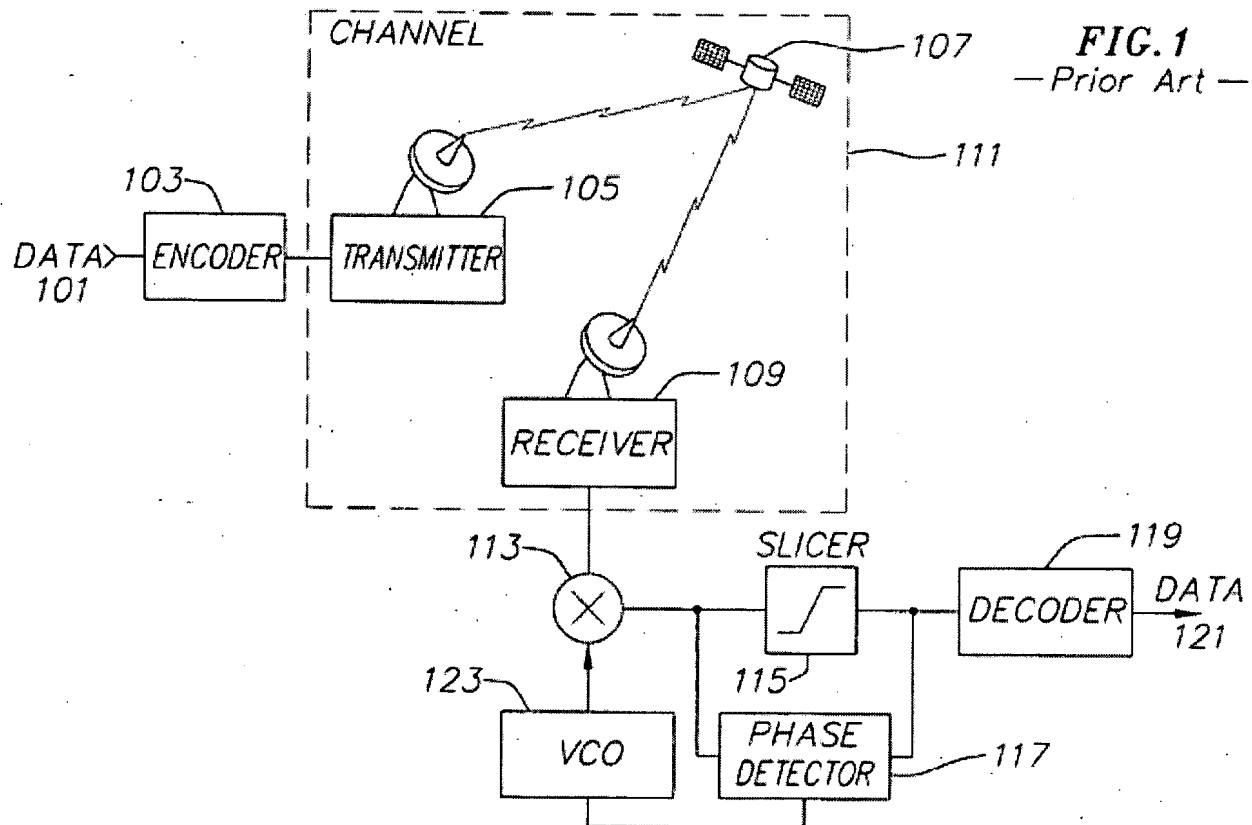
The turbo encoder 200, however, is a parallel concatenated encoder. Turbo encoder 200 comprises two trellis encoders separated by an interleaver 205. Any number of trellis encoders separated by interleavers may be used, but two are shown for sake of simplicity.

The interleaver 205 accepts the data 201 and interleaves or shuffles the data before providing it to the trellis encoder 207. As a result, the data provided by the lower leg of the turbo

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encoder comprising the trellis encoder 207 is out of sequence and must be resequenced. For this reason, switch 303 is added to the Viterbi decoder 301 so that only the symbols from trellis encoder 203 or trellis encoder 207 are used by the phase detector 217 to adjust the controlled oscillator 223. The delay introduced by interleaver 205 makes it impractical for the Viterbi decoder 301 to use symbols from both sides of the turbo encoder 200 without a buffering and delay mechanism at the input of the Viterbi decoder. Switch 303 will select every other symbol. Either a symbol from trellis encoder 203 will be selected or a symbol from trellis encoder 207 will be selected by switch 303.

Figure 4 is a graphical illustration of a communication system according to an embodiment of the invention. In Figure 4, the turbo encoder 403 has been modified by placing an inverse interleaver in series with trellis encoder 207. The inverse interleaver 401 unscrambles the order of the data which had been scrambled by the interleaver 205, after it has been trellis encoded. By utilizing inverse interleaver 401, every symbol can be used by the Viterbi decoder 301 in order to synchronize the frequency of the VCO 223.





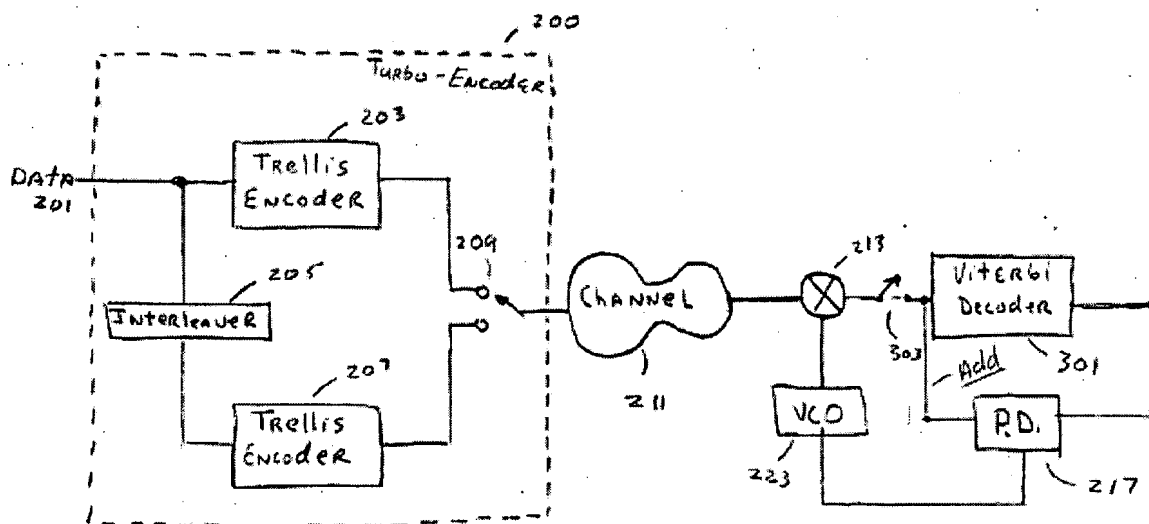
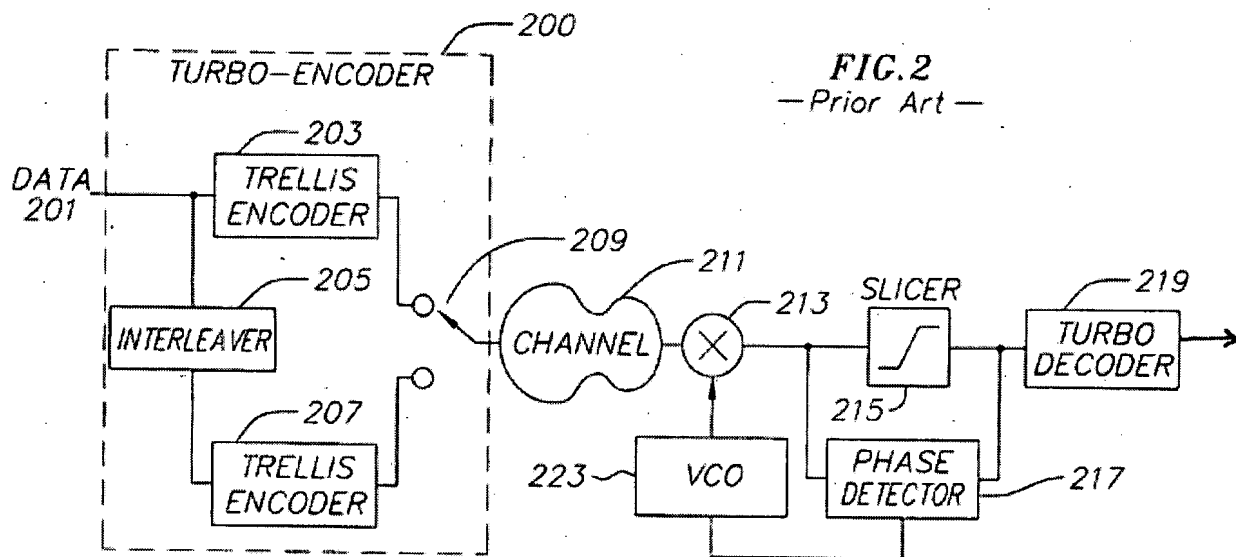


Figure 3

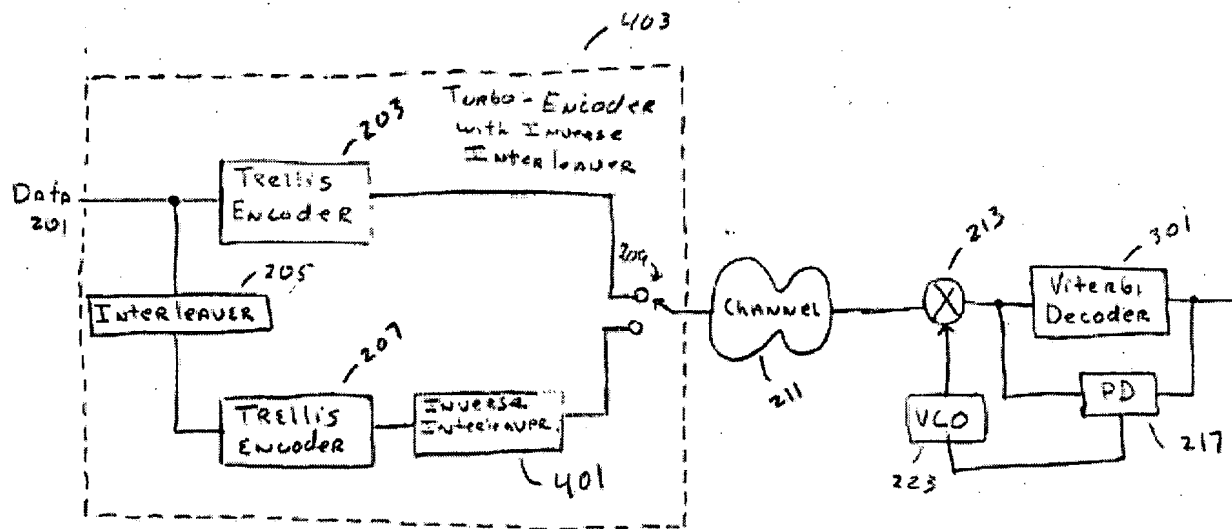


Figure #4

It is clear from the detail description and the drawings that the invention is to substitute the slicer in figure 2 by a Viterbi decoder because "Turbo encoder 200 is a parallel concatenated encoder. Parallel concatenated codes ("turbo codes") allow communications systems to operate near the Shannon capacity. However, when operating in this region, the signal to noise ratio may be very low. This low signal to noise ratio ( $E_s/N_0$ ) can make synchronization with a received signal difficult"....."A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer). In the embodiment illustrated in FIG. 3, future data is not available, so the Viterbi decoder 301 will examine past and present data in order to produce a symbol, which is more likely to be accurate than one determined by a slicer mechanism such as illustrated in FIG. 2".

The reference used by the Examiner under statutory bar 102(b) of 35 USC (Mottier "Influence of tentative decisions provided by a Turbo-decoder on the carrier synchronization: Application to 64-QAM signals", COST 254 Workshop on Emerging Techniques for Communication Terminals, Toulouse France July 7-9, 1997, pages 326-330) present the same idea: Figure 1 present the use of the classical slicer in the carrier synchronization, similar to the figure 2 of the present Application

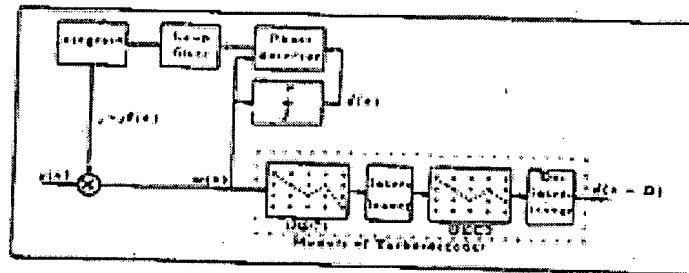


Fig. 1. Classical concatenation of a carrier recovery loop and a Turbo-decoder.

Because the turbo decoder need to work a low SNR the slicer have to be improved (see abstract), so this paper present the idea of the substitution of the slicer by a Viterbi decoder DEC1 in figure 3:

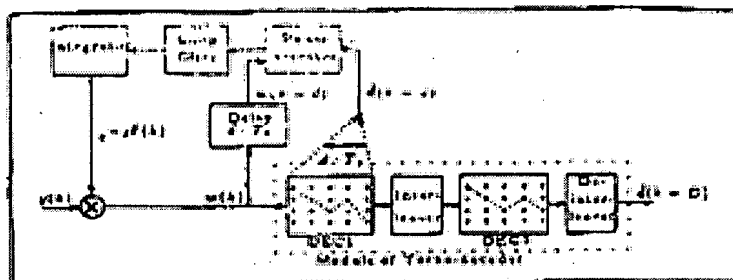


Fig. 3. Carrier recovery loop using tentative decisions from a Turbo-decoder.

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The reference also indicated why is using only one Viterbi decoder DEC1 instead of the output of the Viterbi decoder, because of the delay introduced by the turbo decoder (see section 3.2 "Delay insertion").

So it is clear from this presentation that the reference of Mottier clearly anticipated the idea of the present invention.

As indicated by the Applicant a "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"

So after a very carefully review and consideration of the specification and drawings of the present application and the reference used for the rejection it is clear the rejection is proper and should be maintained.

It is also important to considerate the reference of Moller also provide detail simulations of the performance of the system in comparison with slicer, Viterbi decoder and also using the output of the turbo coder.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 62-67, 72-77, 82-86, 91-94, 99-101, 106-108 and 113 are rejected under 35 U.S.C. 102(b) as being anticipated by Mottier ("Influence of tentative decisions provided by a Turbo-decoder on the carrier synchronization: Application to 64-QAM

signals", COST 254 Workshop on Emerging Techniques for Communication Terminals, Toulouse France July 7-9, 1997, pages 326-330).

Regarding claims 62 and 72, Mottier discloses an input, coupled to a communication channel, that is operable to receive a signal (figure 3  $y(k)$  sections 2 and 3, pages 327-328); a synchronization module that includes a Viterbi decoder, a phase detector, and a voltage controlled oscillator, wherein the synchronization module is operable to recover a first symbol, a second symbol, and a third symbol from the signal (figure 3 sections 2 and 3, pages 327-328); the first symbol is followed by the second symbol (figure 3 sections 2 and 3, pages 327-328); and the second symbol is followed by the third symbol (figure 3 sections 2 and 3, pages 327-328); and a turbo decoder that is operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein (figure 3 "turbo decoder" sections 2 and 3, pages 327-328).

Regarding claims 63 and 73, Mottier discloses claims 62 and 72, Mottier also discloses a multiplier, whose mixing frequency is governed by the voltage controlled oscillator, that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal frequency (figure 3 sections 2 and 3, pages 327-328 multiplier after  $y(k)$ ).

Regarding claims 64 and 74, Mottier discloses claims 62 and 72, Mottier also discloses that the Viterbi decoder is operable to consider the first symbol when estimating the second symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent

to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"; and the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)").

Regarding claims 65 and 75, Mottier discloses claims 62 and 72, Mottier also discloses a multiplier, whose mixing frequency is governed by the voltage controlled oscillator, that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 sections 2 and 3, pages 327-328 multiplier after  $y(k)$ ); and wherein: the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of

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the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"; and the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, as performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 "phase detector").

Regarding claims 66 and 76, Mottier discloses claims 62 and 72, Mottier also discloses a multiplier, whose mixing frequency is governed by the voltage controlled oscillator, that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 sections 2 and 3, pages 327-328 multiplier after  $y(k)$ ); and wherein: the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"; the phase detector is operable to employ at

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least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, as performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 "phase detector"); and the adjustment of the voltage controlled oscillator is operable to make the mixing frequency to be substantially equal to the carrier frequency of the signal (figure 3 sections 2 and 3, pages 327-328 output of the phase detector).

Regarding claims 67 and 77, Mottier discloses claims 62 and 72, Mottier also discloses a multiplier, whose mixing frequency is governed by the voltage controlled oscillator, that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 sections 2 and 3, pages 327-328 multiplier after  $y(k)$ ); and wherein the third symbol output from the multiplier is provided simultaneously to both the Viterbi decoder and the phase detector (figure 3 sections 2 and 3, pages 327-328 after multiplier after  $y(k)$  the symbols are provided to the phase detector and to the Viterbi decoder); the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder); and the phase detector is operable to compare the third symbol output from the multiplier and the estimate of the third symbol as made by the Viterbi decoder to determine whether recovery of symbols from the signal, as performed by the synchronization module, is lagging or leading



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actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 phase detector).

Regarding claim 82, Mottier discloses an input, coupled to a communication channel, that is operable to receive a signal (figure 3  $y(k)$  sections 2 and 3, pages 327-328); a multiplier that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 sections 2 and 3, pages 327-328 multiplier after  $y(k)$ ); a synchronization module that includes a Viterbi decoder, a phase detector, and a voltage controlled oscillator (figure 3 sections 2 and 3, pages 327-328), wherein: the Viterbi decoder and the phase detector each receive the mixed signal output from the multiplier (figure 3 sections 2 and 3, pages 327-328 output of the multiplier); the synchronization module is operable to recover a first symbol, a second symbol, and a third symbol from the signal (figure 3 sections 2 and 3, pages 327-328); the first symbol is followed by the second symbol, the second symbol is followed by the third symbol (figure 3 sections 2 and 3, pages 327-328); and the mixing frequency of the multiplier is governed by the voltage controlled oscillator (figure 3 sections 2 and 3, pages 327-328); and a turbo decoder that is operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein (figure 3 sections 2 and 3, pages 327-328 turbo decoder).

Regarding claim 83, Mottier discloses claim 82, Mottier also discloses that the Viterbi decoder is operable to consider the first symbol when estimating the second

symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); and the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)").

Regarding claim 84, Mottier discloses claim 82, Mottier also discloses that the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328); and the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, as performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 "phase detector").

Regarding claim 85, Mottier discloses claim 82, Mottier also discloses that the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, as performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 "phase detector"); and the adjustment of the voltage controlled oscillator is operable to make the mixing frequency to be substantially equal to the carrier frequency of the signal (figure 3 sections 2 and 3, pages 327-328 output of the phase detector).

Regarding claim 86, Mottier discloses claim 82, Mottier also discloses that the third symbol output from the multiplier is provided simultaneously to both the Viterbi decoder and the phase detector (figure 3 sections 2 and 3, pages 327-328 after multiplier after  $y(k)$  the symbols are provided to the phase detector and to the Viterbi decoder); the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this

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is inherent to a Viterbi decoder); and the phase detector is operable to compare the third symbol output from the multiplier and the estimate of the third symbol as made by the Viterbi decoder to determine whether recovery of symbols from the signal, as performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 phase detector).

Regarding claim 91, Mottier discloses receiving a signal from a communication channel (figure 3  $y(k)$  sections 2 and 3, pages 327-328); recovering a first symbol, a second symbol, and a third symbol from the signal from the signal by multiplying the signal by a mixing frequency to match a carrier frequency of the signal and subsequent Viterbi decoding and phase detection of symbols generated by the frequency mixing (figure 3 sections 2 and 3, pages 327-328 multiplier after  $y(k)$ , Viterbi decoder and phase detector), wherein: the multiplied signal is simultaneously provided for Viterbi decoding and phase detection (figure 3 sections 2 and 3, pages 327-328 multiplier after  $y(k)$ , Viterbi decoder and phase detector); the first symbol is followed by the second symbol (figure 3 sections 2 and 3, pages 327-328); and the second symbol is followed by the third symbol (figure 3 sections 2 and 3, pages 327-328 multiplier after  $y(k)$ , Viterbi decoder and phase detector); and when performing Viterbi decoding, considering the first symbol when estimating the second symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi

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decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); when performing Viterbi decoding, considering the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328); and turbo decoding the first symbol, the second symbol, and the third symbol that are recovered from the signal to make best estimates of information bits encoded therein (figure 3 sections 2 and 3, pages 327-328 turbo decoder).

Regarding claim 92, Mottier discloses claim 91, Mottier also discloses employing at least one of the first symbol, the second symbol, and the third symbol when performing phase detection to determine whether recovery of symbols from the signal is lagging or leading actual symbols within the signal (figure 3 sections 2 and 3, pages 327-328 phase detector, multiplier, Viterbi decoder); and adjusting the mixing frequency based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 phase detector).

Regarding claim 93, Mottier discloses claim 91, Mottier also discloses employing at least one of the first symbol, the second symbol, and the third symbol when performing phase detection to determine whether recovery of symbols from the signal is lagging or leading actual symbols within the signal (figure 3 sections 2 and 3, pages 327-328 phase detector, multiplier, Viterbi decoder); adjusting the mixing frequency based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 phase detector); and wherein: the adjustment of the mixing frequency is operable to make the

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mixing frequency to be substantially equal to the carrier frequency, of the signal (figure 3 sections 2 and 3, pages 327-328 carrier synchronization).

Regarding claim 94, Mottier discloses claim 91, Mottier also discloses when performing phase detection, comparing the third symbol output from the multiplying and the estimate of the third symbol as made in accordance with Viterbi decoding to determine whether recovery of symbols from the signal is lagging or leading actual symbols within the signal (figure 3 sections 2 and 3, pages 327-328 phase detector, multiplier and Viterbi decoder); and adjusting the mixing frequency based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 carrier synchronization).

Regarding claims 99 and 106, Mottier discloses an input, coupled to a communication channel, that is operable to receive a signal (figure 3  $y(k)$  sections 2 and 3, pages 327-328); a multiplier that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 multiplier after  $y(k)$  sections 2 and 3, pages 327-328); a synchronization module that includes a Viterbi decoder, a phase detector, and a voltage controlled oscillator (figure 3 multiplier, Viterbi decoder, phase detector, pages 327-328), wherein: the Viterbi decoder and the phase detector each receive the mixed signal output from the multiplier (figure 3 output multiplier input to Viterbi decoder and phase detector, pages 327-328); the synchronization module is operable to recover a first symbol, a second symbol, and a third symbol from the signal (figure 3 multiplier, Viterbi decoder, phase detector, pages 327-328); the first symbol is followed by the second symbol (figure 3 pages 327-328);

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the second symbol is followed by the third symbol (figure 3 pages 327-328); the mixing frequency of the multiplier is governed by the voltage controlled oscillator (figure 3 pages 327-328); the Viterbi decoder is operable to consider the first symbol when estimating the second symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328, see above); and the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, as performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 carrier synchronization); and a turbo decoder that is operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein (figure 3 sections 2 and 3, pages 327-328 turbo decoder).

Regarding claims 100 and 107, Mottier discloses claims 99 and 106, Mottier also discloses that the adjustment of the voltage controlled oscillator is operable to make the

mixing frequency to be substantially equal to the carrier frequency of the signal (figure 3 sections 2 and 3, pages 327-328 carrier synchronization).

Regarding claims 101 and 108, Mottier discloses claims 99 and 106, Mottier also discloses that the third symbol output from the multiplier is provided simultaneously to both the Viterbi decoder and the phase detector (figure 3 sections 2 and 3, pages 327-328 output of the multiplier to the phase detector and the Viterbi decoder).

Regarding claim 113, Mottier discloses an input, coupled to a communication channel, that is operable to receive a signal (figure 3  $y(k)$  sections 2 and 3, pages 327-328); a multiplier that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 multiplier sections 2 and 3, pages 327-328); a synchronization module that includes a Viterbi decoder, a phase detector, and a voltage controlled oscillator (figure 3 multiplier, Viterbi decoder and phase detector sections 2 and 3, pages 327-328), wherein: the Viterbi decoder and the phase detector each receive the mixed signal output from the multiplier (figure 3 the output of the multiplier is sent to the Viterbi decoder and the phase detector sections 2 and 3, pages 327-328); the output of the Viterbi decoder is provided to the phase detector (figure 3 output of Viterbi decoder is sent to the other input of the phase detector sections 2 and 3, pages 327-328); the synchronization module is operable to recover a first symbol, a second symbol, and a third symbol from the signal such that the first symbol is followed by the second symbol and the second symbol is followed by the third symbol (figure 3  $y(k)$  sections 2 and 3, pages 327-328); the Viterbi decoder is operable



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to consider the first symbol when estimating the second symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); and the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, as performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 carrier synchronization sections 2 and 3, pages 327-328); and the adjustment of the mixing frequency by the voltage controlled oscillator is operable to make the mixing frequency to be substantially equal to the carrier frequency of the signal (figure 3 carrier synchronization sections 2 and 3, pages 327-328); and a turbo decoder that is

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operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein (figure 3 turbo decoder sections 2 and 3, pages 327-328).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 68, 70, 71, 78, 80, 81, 87, 89, 90, 95, 97, 98, 102, 104, 105, 109, 111, 112, 114 and 115 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mottier as applied to claims 62, 72 and 82 above, and further in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 68, 78, 87, 95, 102, 109 and 114, Mottier discloses claims 62, 72, 82, 91, 99, 106 and 113, Mottier doesn't specifically disclose that the communication device is coupled to at least one additional communication device via the communication channel; the at least one additional communication device includes a turbo encoder that is operable to encode at least one information bit thereby generating at least one of the first symbol, the second symbol, and the third symbol of the signal; and the at least one additional communication device is operable to launch the signal into the communication channel. AAPA discloses that the communication device is coupled to at least one additional communication device via the communication channel (figure 2 page 3 line 34 to page 4 line 6); the at least one additional communication

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device includes a turbo encoder that is operable to encode at least one information bit thereby generating at least one of the first symbol, the second symbol, and the third symbol of the signal (figure 2 page 3 line 34 to page 4 line 6); and the at least one additional communication device is operable to launch the signal into the communication channel (figure 2 page 3 line 34 to page 4 line 6). Mottier and AAPA teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the carrier synchronization technique disclosed by Mottier with the system disclosed by AAPA. The suggestion/motivation for doing so would have been to use an effective synchronization at very low SNR (Mottier abstract).

Regarding claims 70, 80, 89, 97, 104, 111 and 115, Mottier discloses claims 62, 72, 82, 91, 96, 106 and 113, Mottier doesn't specifically disclose that the signal is received by the communication device via a communication channel that couples the communication device to a relay satellite. AAPA discloses that the signal is received by the communication device via a communication channel that couples the communication device to a relay satellite (figures 1 page 3 lines 15-24). Mottier and AAPA teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the carrier synchronization technique disclosed by Mottier with the system disclosed by AAPA. The suggestion/motivation for

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doing so would have been to use and effective synchronization at very low SNR (Mottier abstract).

Regarding claims 71, 81, 90, 98, 105 and 112, Mottier discloses claims 62, 72, 82, 91, 99 and 106, Mottier doesn't specifically disclose that the communication device is coupled to at least one additional communication device via the communication channel (figures 1 page 3 lines 15-24); the communication channel includes a relay satellite (figures 1 page 3 lines 15-24); the communication device is a satellite communication receiver (figures 1 page 3 lines 15-24); and the at least one additional communication device is a communication transmitter (figures 1 page 3 lines 15-24). Mottier and AAPA teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the carrier synchronization technique disclosed by Mottier with the system discloses by AAPA. The suggestion/motivation for doing so would have been to use and effective synchronization at very low SNR (Mottier abstract).

Claims 69, 79, 88, 96, 103, 110 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mottier as applied to claims 62 and 72 above, in view of AAPA, and further in view of Robertson et al., "Bandwidth-Efficient Turbo Trellis-coded Modulation Using Punctured Component Codes," IEEE Journal on Selected Areas in Communications; 02/1998, p.p. 206-218, Vol. 16, No. 2).

Regarding claims 69, 79, 88, 96, 103 and 110, Mottier discloses claims 62, 72, 82, 91, 96 and 106, Mottier doesn't specifically disclose that the communication device

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is coupled to at least one additional communication device via the communication channel; the at least one additional communication device includes a turbo encoder that is operable to encode data thereby generating the first symbol, the second symbol, and the third symbol of the signal; the turbo encoder includes: a first trellis encoder that is operable to encode the data thereby generating first encoded data; an interleaver that is operable to interleave the data thereby generating interleaved data; a second trellis encoder that is operable to encode the interleaved data thereby generating interleaved encoded data; an inverse interleaver that is operable to unscramble the interleaved encoded data that has been generated by the second trellis encoder thereby generating second encoded data; a switch that is operable alternatively to select symbols from the first encoded data and the second encoded data; and the at least one additional communication device is operable to launch the signal into the communication channel.

AAPA discloses the communication device is coupled to at least one additional communication device via the communication channel (figure 2 page 3 line 34 to page 4 line 6); the at least one additional communication device includes a turbo encoder that is operable to encode data thereby generating the first symbol, the second symbol, and the third symbol of the signal (figure 2 page 3 line 34 to page 4 line 6); the turbo encoder includes: a first trellis encoder that is operable to encode the data thereby generating first encoded data (figure 2 page 3 line 34 to page 4 line 6); an interleaver that is operable to interleave the data thereby generating interleaved data (figure 2 page 3 line 34 to page 4 line 6); a second trellis encoder that is operable to encode the interleaved data thereby generating interleaved encoded data (figure 2 page 3 line 34 to

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page 4 line 6); a switch that is operable alternatively to select symbols from the first encoded data and the second encoded data (figure 2 page 3 line 34 to page 4 line 6); and the at least one additional communication device is operable to launch the signal into the communication channel (figure 2 page 3 line 34 to page 4 line 6). Mottier and AAPA teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the carrier synchronization technique disclosed by Mottier with the system disclosed by AAPA. The suggestion/motivation for doing so would have been to use an effective synchronization at very low SNR (Mottier abstract). Robertson teaches that the turbo-coded transmitted signals comprise interleaving and de-interleaving of the turbo encoded signals before transmission (figure 2 and 2 page 208 section II the encoder). Mottier, AAPA and Roberson teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the interleaving and de-interleaving of the turbo encoded signals before transmission disclosed by Roberson with the carrier recovery scheme disclosed by Mottier and AAPA. The suggestion/motivation for doing so would have been to ensure that the ordering of the two information bits partly defining each symbol corresponds to that of the first encoder (Roberson page 208 section II. A) and to reduce the latency of the turbo decoder.

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***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Juan Alberto Torres  
08-31-2007

  
**MOHAMMED GHAYOUR**  
**SUPERVISORY PATENT EXAMINER**